# On Aging Of Key Transistor Device Parameters

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***Abstract*** - Aging of key transistor device parameters are described to help explain their overall reliability, relationships to device junction degradation, and to aid in predicting parameter degradation. This work gives a number simple formulations that help provide insight into why key device transistor parameters age. This is provided in both the bipolar and FET (Field-Effect Transistor) case. Although the formulations are simple, they illustrate the important role that leakage current plays in aging of key device parameters for bipolar and FET transistors.

## 1. Introduction

In this paper we are primarily concerned with reliability of key transistor device parameters. In the bipolar case for the common-emitter configuration, the key transistor parameter studied is beta aging showing it to be directly proportional to the fractional change in the base-emitter leakage current. In the FET (Field-Effect Transistor) case, the key transistor parameter considered is transconductance aging that results from a change in the drain-source resistance and gate leakage current. We provide aging expressions that account for the time degradation of these parameters found in life test. These expressions provide insight into degradation that links aging to junction temperature dependent mechanisms. Some typical life test data on both HBTs (Hetrojunction Bipolar Transistor) and MESFETs (Metal Semiconductor Field-Effect Transistor) are presented from experiments to illustrate these results.

### Bipolar Beta Aging Mechanism

There are two main bipolar aging mechanisms, increase in emitter ohmic contact resistance and degradation due to base leakage currents. Transitor gain ($\beta$) degradation, commonly expressed by beta change, is the primary reliability concern here. The simple expression shown here illustrate that the base leakage current correlates well to degradation of the transistor gain (beta parameter) on life test (see Eq. 9). Typical data are illustrated in Figure 1. Since beta ($\beta$) is given by $I_{ce}/I_{be}$ (collector current/base current) in the common-emitter configuration, any degradation in $I_{be}$ will degrade beta. In our life test study, a Gummel plot in Figure 2 showed increases in emitter-base leakage current over time. However, no noticeable increases in emitter-collector current were observed. Additionally, a number of devices were tested where no increase in reverse bias base-collector current was found. This is fairly typical, other authors have observed similar transistor aging [1-4] behavior.

In this section, a simple model is developed that helps explain leakage current to beta degradation over time. The model goes further in describing the degradation's time dependence.

Consider a change in the beta for the common emitter configuration

$$\beta\ (t) = \beta_O - \left|\Delta\beta\ (t)\right| \qquad (1)$$

where beta $\beta_o$ is the initial value (prior to aging) of $I_{ce}/I_{be}$. Looking at it's time dependence for the function $\Delta\beta(t)$ we first consider

$$\dot{\beta}(t) = \frac{d\beta}{dt} = \beta_o\left(\frac{\dot{I}_{ce}}{Ice} - \frac{\dot{I}_{be}}{Ibe}\right) \qquad (2)$$

Approximating d/dt by $\Delta/\Delta t$ with $\Delta t$ canceling out then

$$\Delta\beta(t) \cong -\beta_o\left(\frac{\Delta I_{be}(t)}{Ibe}\right) \qquad (3)$$

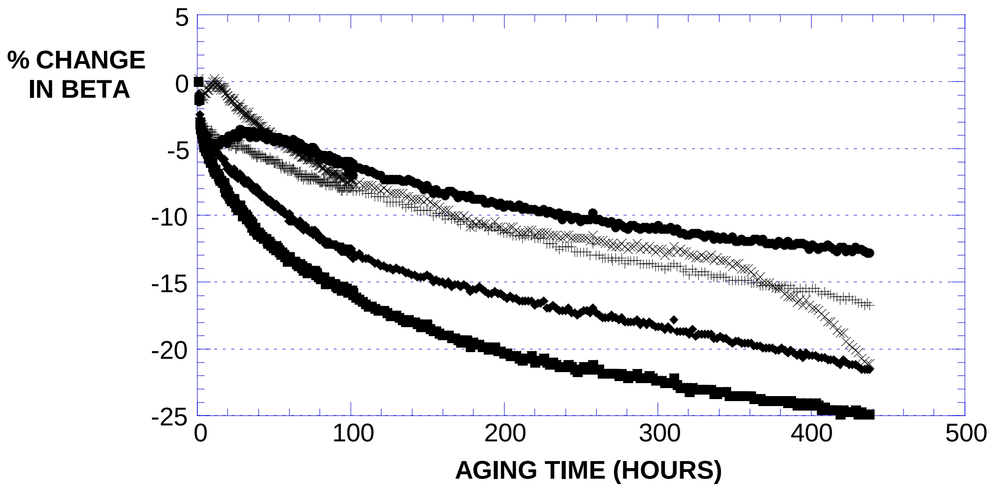


**Figure 1** Life test data on C-doped MBE HBT devices at 235C at 10kA/Cm$^2$

In the above equation, we have approximated $\Delta I_{ce}$ as zero as this parameter commonly shows little change over time.

Although the above formulation is reasonably simple, it illustrates that Beta degradation is directly proportional to the fractional change in the base-emitter leakage current. This mechanism is reasonably well known (while perhaps to our knowledge not as simply shown).

**A Simple Capacitor Model For Describing Base-Emitter Leakage**

When a transistor is first turned on, electrons penetrate into the base bulk gradually. They reach the collector only after a certain delay time $\tau_d$. The collector current then starts to build related to the current diffusion rate. Concurrent with the increase of collector current, excess charges builds up in the base. As a first approximation the collector current and excess charges increase in an exponential manner with a time constant $\tau_b$ [5]. This transient is modeled as the process of charging a capacitor in the simplest of RC circuits shown in Figure 3 [5]. We use this approximation to provide a simple model for base leakage. The steady-state value of charge build up in the base-emitter bulk $Q_k$ is then

$$Q_k=(Q_{be})_k \cong (C_{be}V_{be})_k = (C_{be}\,(I_{be}R_{be}))_k = (I_{be}\ \tau_b)_\kappa \qquad (4)$$

where $\tau_b = R_{be}C_{be}$ is the time constant for steady-state excess charges in the base-emitter junction ($\tau_b >> \tau_d$). As discussed above, this junction leakage primarily contributes to aging effects. Along with this bulk effect are parasitic surface charging ($Q_s$) and surface leakage contributions. For simplicity we feel it is reasonable to assume these effects can be similarly treated to undergo capacitive like charging and leakage. Thus in this view the surface leakage can be expressed as

$$Q_s=(Q_{be})_s \cong (C_{be}V_{be})_s = (C_{be}\,(I_{be}R_{be}))_s = (I_{be}\,\tau_b)_\sigma \qquad (5)$$

The total charging at the base with these two components is then

$$Q_{be}=Q_s+Q_k \qquad (6)$$

As the transistor ages $Q_{be}$ increase along with $I_b$. Some of the reasons for increases in $Q_{be}$ over time could be due to increases in impurities and defects in the base surface and bulk regions due to operating stresses.

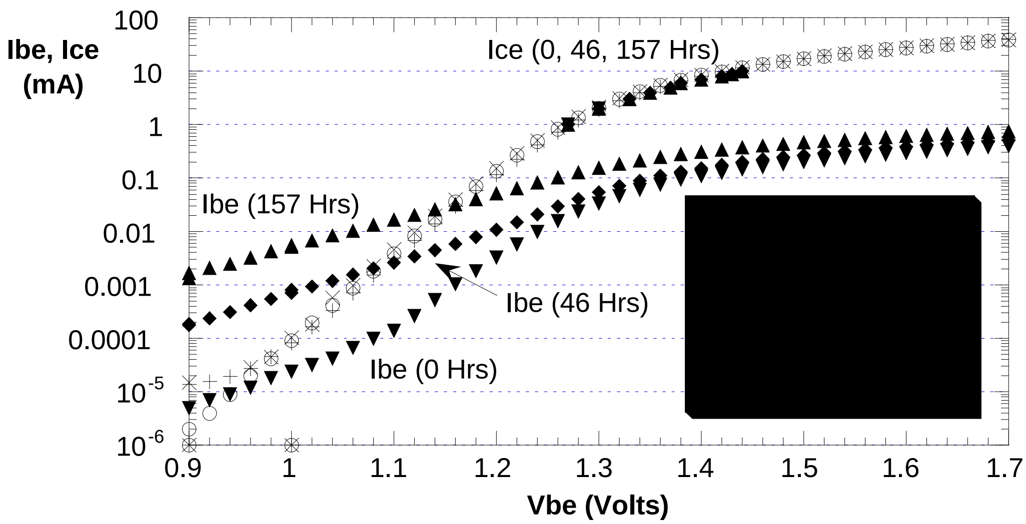


**Figure 2** HBT Gummel plot results ($I_{ce}$ 12 ma) of life test devices in Fig. 1

This causes an increase in electron scattering increasing the probability for trapping and charging and eventual recombination in the base contributing to increased leakage. In the capacitve model shown in Figure 3, incremental changes are

$$dQ=C\,dV=C\,R\,dI = \tau\,dI \qquad (7)$$

where Q, V, and I are treated as time varying with age. This implies then

$$\Delta\beta(t) \cong -\beta_o\left(\frac{\Delta I_{be}(t)}{Ibe}\right) = -\beta_o\left(\frac{\Delta Q_{be}(t)}{Qbe}\right)$$

$$= -\beta_o\left(\frac{\Delta V_{be}(t)}{Vbe}\right) \qquad (8)$$

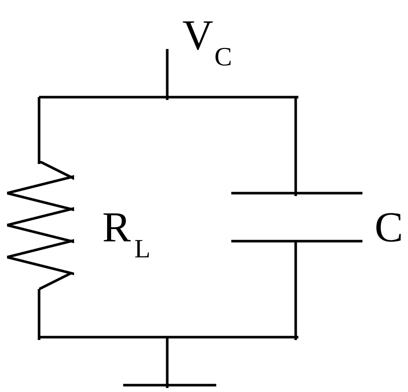


**Figure 3** Capacitive leakage model

Thus, in this simple view, change in beta is proportional to the fractional change in the base-emitter leakage current, charge, and voltage.

Experimentally, we have found that the Beta degradation, as displayed graphically in Figure 1, follows the following aging equation,

$$\frac{\Delta\beta(t)}{\beta_o} = \frac{\Delta I_{be}(t)}{Ibe} = A\ Log(1 + B\ time) \tag{9}$$

In section, IV, we will provide an explanation to this observed log(time) aging that is consistent with the above modeling results and observed MESFET data discussed below.

**II. FET Transconductance Degradation**

Just as important as understanding Beta gain degradation in the Bipolar case, the transconductance parameter is a key factor in FET reliability. In this section, we provide a simple formulation for transconductance degradation over time to help understand aging in FET devices. Similar to the Beta expression in (1), we start by looking at the transconductance $g_m$ as a function of time as

$$g_m(t) = g_o - \left|\Delta g_m(t)\right| \tag{10}$$

where $g_o$, the initial value is taken in the flat portion of the transconductance curve as

$$g_o = \left(\frac{dI_{DS}}{V_{GS}}\right)_{V_{DS}} \approx \frac{I_{DS}}{V_{GS} - V_o} \tag{11}$$

Here we use the flat portion of the curve for simplicity, similar results will follow for other portions of the curve. The time-dependent function $\Delta g_m(t)$ is found from its time derivative as

$$\dot{g}_m(t) = \frac{dg_m}{dt} = \frac{d}{dt}\left(\frac{I_{DS}}{V_{GS} - V_o}\right)$$

$$= g_{m_o}\left(\frac{\dot{I}_{DS}}{I_{DS}} - \frac{\dot{V}_{GS}}{V_{GS} - V_o}\right) \tag{12}$$

Assuming that the drain-source current change goes as $dI/dt \sim (V/R^2)(dR/dt)$ with $V_{DS}$ constant and Voltage-gate change $dV_{GS}/dt \sim d/dt(IR) = RdI_{GS}/dt$.

Approximating d/dt by $\Delta/\Delta t$ with $\Delta t$ canceling out then

$$\Delta g_m(t) = g_{o_o}\left(\frac{\Delta R_{DS}}{R_{DS}} - \frac{\Delta I_{GS}}{I_{GS} - I_{GS_O}}\right) \tag{13}$$

Although the above formulation is reasonably simple (not found elsewhere to our knowledge), it illustrates that transconductance aging results from a change in the drain-source resistance and/or gate leakage. These mechanisms are known. However, leakage current in the FET is not as often considered, as resistance aging dominates.

In the case of $R_{DS}$ change, resistance is related to scattering inside the drain-source channel where $\Delta R_{DS}/R_{DS} = \Delta\rho_{DS}/\rho_{DS} = \Delta l_{DS}/l_{DS}$ . Here $\rho$ is the resistivity, and l is the average mean free path the electrons travel in the channel between collisions. This distance decreases as aging occurs and more defects occur in the channel causing increased scattering.

At this point, we wish to point out that similar to Beta degradation, a mechanism that we have modeled as dominated by gate leakage, MESFET gate leakage has experimentally displayed in Figure 4 to follows a log(time) aging form given in the MESFET as

$$\frac{\Delta I_{GS}(t)}{I_{GS}} = A\ Log(1 + B\ time) \tag{14}$$

The gate leakage has been fitted to this log(time) model and the results are displayed in Fig. 4. Log(time) aging phenomena are well know. In the next section we discuss its relevance to the leakage mechanism.

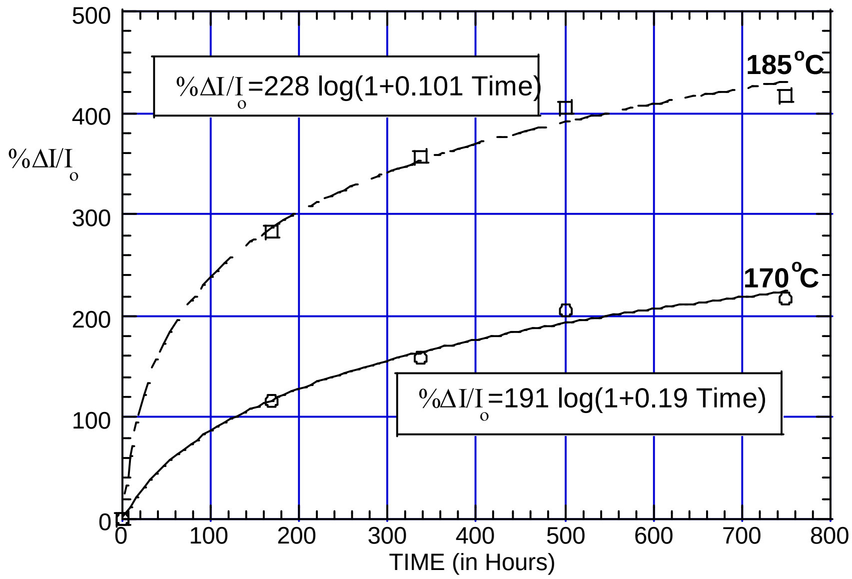


**Fig. 4** Life test data of gate-source MESFET leakage current over time fitted to Log(time) aging model. Temperatures are ambient, junction rise is about 30ºC.

**Log(time) Aging and Capacitive Type Leakage**

Log(time) aging is related to Arrhenius degradation processes. This relationship has been previously described by a Thermally Activated Time-dependent (TAT) model [6,7]. This model has the general form given in Equation (9). However, the model allows one to identify the values of A and B for the particular physical situation. For the case of a leaky capacitor as presented in Figure 3 the results found for current leakage over time and temperature are [8,9,10]

$$\Delta I \cong \frac{K_B T}{\tau\, \Delta V_c}\ \ln[1+\frac{\nu(T)\ \tau\, \Delta V_c}{K_B T}\ t] \qquad (15)$$

Here $K_B$ is Boltzmann's constant, T is temperature, $\tau$ is the RC time constant, $\Delta V_C$ is a critical voltage at which catastrophic problems occur and $\nu(T)$ is the Arrhenius expression

$$\nu(T) = \nu_o \exp\left(-\frac{E_a}{K_B T}\right) \qquad (16)$$

and $\nu_o$ represents a characteristic frequency for the Arrhenius Mechanism

Here we have used this model to help link the leakage expression in (9) and (15) to the log(time) aging results observed in Figure 1 and 4 for Beta degradation and gate leakage. We note that in (21) the leading term in front of mathematical log indicates that leakage is proportional to temperature and inversely proportional to the capacitive charging time constant and the critical voltage. The critical voltage is essentially the breakdown voltage. The model indicates that design parameters of breakdown voltage and $R_L C$ (=$\tau$) values can help control leakage associated with aging.

Therefore, we see the key aging design parameters are as follows:

- Key Aging Transistor Design Parameter
  - Base RC time constant (transient behavior)
  - Critical power - power at which transistor goes catastrophic
  - Channel resistivity/scattering properties (FET case)
- Suggested Method
  - Measure transient behavior and correlate to aging.

- Understand critical power as a function of design.

## IV. Summary

Aging of key transistor device parameter for the Bipolar and FET case have been described. Leakage have been expressed as leaky capacitors and relationships established to aging. In the bipolar case for the common-emitter configuration, we find that transistor beta aging is directly proportional to the fractional change in the base-emitter leakage current. In the FET case, transconductance aging results from a change in the drain-source resistance and gate leakage. This modeling also helps explain their observed log(time) degradation of these parameters observed on life test. We presented simple formulations to help understand this degradation that links this aging to junction temperature dependent leakage current mechanisms. We presented life test data that is representative of typical aging on both HBTs and MESFETs. Additionally, we used a TAT model to link these results with experimentally observed log(time) degradation. Such formulations are important in the understanding of transistor reliability.

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